In re Patent Application of
BUSSON ET AL.
Serial No. **09/827,306**
Filed: **APRIL 5, 2001**

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application. By this amendment, various claims have been amended to eliminate minor informalities contained therein. Claims 11-57 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Invention

As shown in FIGS. 1 and 2, for example, the disclosed invention is directed to a tuner, which can be integrated on a silicon substrate, while avoiding saturation of the various elements of the tuner. The tuner includes an analog block, a digital block, and an analog/digital conversion stage connected therebetween. The analog block includes a first attenuator/controlled-gain amplifier stage connected upstream to a frequency transposition stage. The overall mean power of the entire signal received by the tuner is calculated during initialization. This overall calculated power is compared in the digital block with a first reference value corresponding to a power desired at a location of the analog block. The gain of the first attenuator/amplifier stage is adjusted such as to minimize the deviation between the overall calculated power and the reference value. In normal operation, one of the channels of the signal received is selected, with the gain of the first attenuator/amplifier stage being fixed.

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II. The Claims are Patentable

Claims 11-57 were rejected in view of Ciccarelli et al. (U.S. Patent No. 6,498,926) for the reasons set forth on pages 2-8 of the Office Action. Applicants contend that Claims 11-57 clearly define over the cited reference, and in view of the following remarks, favorable reconsideration of the rejection under 35 U.S.C. §102 is requested.

Independent Claim 1 at least includes comparing the calculated overall power in the digital circuit with a first reference value corresponding to a desired power at a location in the analog circuit, and adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value. Similarly, independent Claim 22 includes adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and a first reference value corresponding to a desired power at a location in the analog circuit.

Also, independent Claims 33 and 46 at least include a digital circuit connected to the analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of the first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired power at a location in the analog circuit.

It is these combinations of features which are not fairly taught or suggested in the cited reference and which patentably define over the cited reference.

The Examiner has relied on the Ciccarelli et al. patent as allegedly disclosing each and every feature of the

claimed invention. The Ciccarelli et al. patent is directed to a programmable linear receiver which provides the required level of system performance at reduced power consumption. The receiver minimizes power consumption based on measurement of the non-linearity in the output signal from the receiver. The amount of non-linearity can be measured by the received-signal-strength-indicator (RSSI) slope or energy-per-chip-to-noise-ratio (Ec/Io) measurement. The RSSI slope is the ratio of the change in the output signal plus intermodulation to the change in the input signal. The input signal is periodically increased by a predetermined level and the output signal from the receiver is measured.

However, the Examiner has misinterpreted and/or mischaracterized the actual teachings of the reference as power measurements in the Ciccarelli et al. system/method are used to adjust the input-referred third-order intercept (IIP3) operating point of various components. Indeed, there is no disclosure of adjusting the gain of the amplifier stage based upon a deviation/comparison between the calculated overall power and a first reference value corresponding to a desired power at a location in the analog circuit, as claimed.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

There is simply no teaching or suggestion in the cited reference to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited reference does not disclose

or fairly suggests the invention as set forth in Claims 11, 22, 33 and 46. Thus, the rejection under 35 U.S.C. §102(e) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number **571-273-8300** to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 27th day of October, 2005.

Sandra Kemp